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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,870	01/08/2002	Peer Johannsen	1454.1210	8728

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,870	JOHANNSEN, PEER	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8 and 9* is/are rejected.

7)☒ Claim(s) *3-7 and 10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This is a response to the amendment filed on 7/14/03. The previous rejections have been withdrawn. New grounds of rejections have been cited in this office action in view of newly discovered prior art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-2, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohara (USP 5517132) Who discloses a method/tool comprising:

(Claim 1) determining, for each property of a non-reduced RTL model a reduced RTL for a design specification by reducing widths of signal occurring in the non-reduced RTL model of the specification (fig 9, c8: 61+) for a design specification, the reduced RTL model retaining the signal property of the non-reduced RTL model; and

subjecting the reduce RTL model to a property checking process (in fig 1-27)

(Claim 8) a pre-property checking unit (in fig 1-27) to reduce width of signal occurring in a non-reduced RTL model of an input design specification for a digital circuit, to produce a reduced RTL model retaining signal properties of the non-reduced RTL model (c8: 61+)

a verification engine couple to the pre-property checking unit to verify whether signal properties of the non-reduced RTL model hold for the reduce RTL model (fig 1-2, 9-11, 13-16, 24)

(Claim 2) determining the design specification and properties of a digital circuit design prior to said determining of the reduced RTL model (fig 1-27); and

Synthesizing an RTL netlist of high level primitives (abstract/background/summary/fig 9, 13-16, 18) so that the digital circuit is defined as an interconnection of control and data path portions where signal of a width n (c8: 61+) are determined such that n ∈ N+ wherein N+ is a positive integer and bit vector of respective lengths each determine a signal value (test mode/signals in fig 18)

(Claim 9) a front-end unit (fig 1-2/9/13-16/24, the front-end unit is the unit(s) interfacing design/specification/description/behavior/chip/VHDL/data base/input) coupling to said pre-property checking unit to receive input data relating to a design specification and properties characteristics of a design of a design to be verified, to provide an RTL net list (fig 9) of the design specification and properties characteristics, so that the digital circuit is defined as an interconnection of control and data path portions where signal of a width n (c8: 61+) are determined such that n ∈ N+ wherein N+ is a positive integer and bit vectors (test mode/signals in fig 18) of respective lengths determine signal value.

2. Claims 1, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Takemura et al (USP 6523153) Who discloses a method/tool comprising:

(Claim 1) determining, for each property of a non-reduced RTL model a reduced RTL for a design specification by reducing widths of signal occurring in the non-reduced RTL model of the specification (fig 2-4) for a design specification, the reduced RTL model retaining the signal property of the non-reduced RTL model; and

subjecting the reduce RTL model to a property checking process (abstract/background/summary/ fig 1-8)

(Claim 8) a pre-property checking unit (in fig 1-8) to reduce width of signal occurring in a non-reduced RTL model of an input design specification for a digital circuit, to produce a reduced RTL model retaining signal properties of the non-reduced RTL model (fig 2-4);

a verification engine couple to the pre-property checking unit to verify whether signal properties of the non-reduced RTL model hold for the reduce RTL model (abstract/background/summary/ fig 1-8).

3. Claims 1-2, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Sharma et al (USP 5841663) Who discloses a method/tool comprising:

(Claim 1) determining, for each property of a non-reduced RTL model a reduced RTL for a design specification by reducing widths of signal occurring in the non-reduced RTL model of the

specification (fig 1, 4, 7-8, 13-14, 16 and c7: 51-53) for a design specification, the reduced RTL model retaining the signal property of the non-reduced RTL model; and

subjecting the reduce RTL model to a property checking process (abstract/background/summary/ fig 1-16)

(Claim 8) a pre-property checking unit to reduce width of signal (fig 1, 4, 7-8, 13-14, 16 and c7: 51-53) occurring in a non-reduced RTL model of an input design specification for a digital circuit, to produce a reduced RTL model retaining signal properties of the non-reduced RTL model;

a verification engine couple to the pre-property checking unit to verify whether signal properties of the non-reduced RTL model hold for the reduce RTL model (background/summary/ fig 1-16).

(Claim 2) determining the design specification and properties of a digital circuit design prior to said determining of the reduced RTL model (fig 1-16); and

Synthesizing an RTL netlist of high level primitives (abstract/background/summary/fig 1/8/16) so that the digital circuit is defined as an interconnection of control and data path portions where signal of a width n are determined such that $n \in N+$ wherein N+ is a positive integer and bit vector of respective lengths each determine a signal value (c4, 6)

(Claim 9) a front-end unit (fig 1/4/7-8/13/16, the front-end unit is the unit(s) interfacing design/specification/description/behavior/chip/VHDL/data base/input) coupling to said pre-property checking unit to receive input data relating to a design specification and properties characteristics of a design of a design to be verified, to provide an RTL net list (fig 1, 16) of the design specification and properties characteristics, so that the digital circuit is defined as an interconnection of control and data path portions where signal of a width n are determined such that $n \in N+$ wherein N+ is a positive integer and bit vectors of respective lengths determine signal value (c4, 6).

Allowable Subject Matter

Claims 3-7, 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-7, 10-13 would be allowable because the prior art does not teach or suggest: the limitations in: Claim 3, lines 2-7 and similarly recited claim 10, line 2-10;

Claim 5, lines 2-10 and similarly recited claim 12, line 2-10.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is (703) 305-5662. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (703) 308-1323. The fax number for the organization handling this application is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Paul Dinh
Patent Examiner
August 4, 2003